



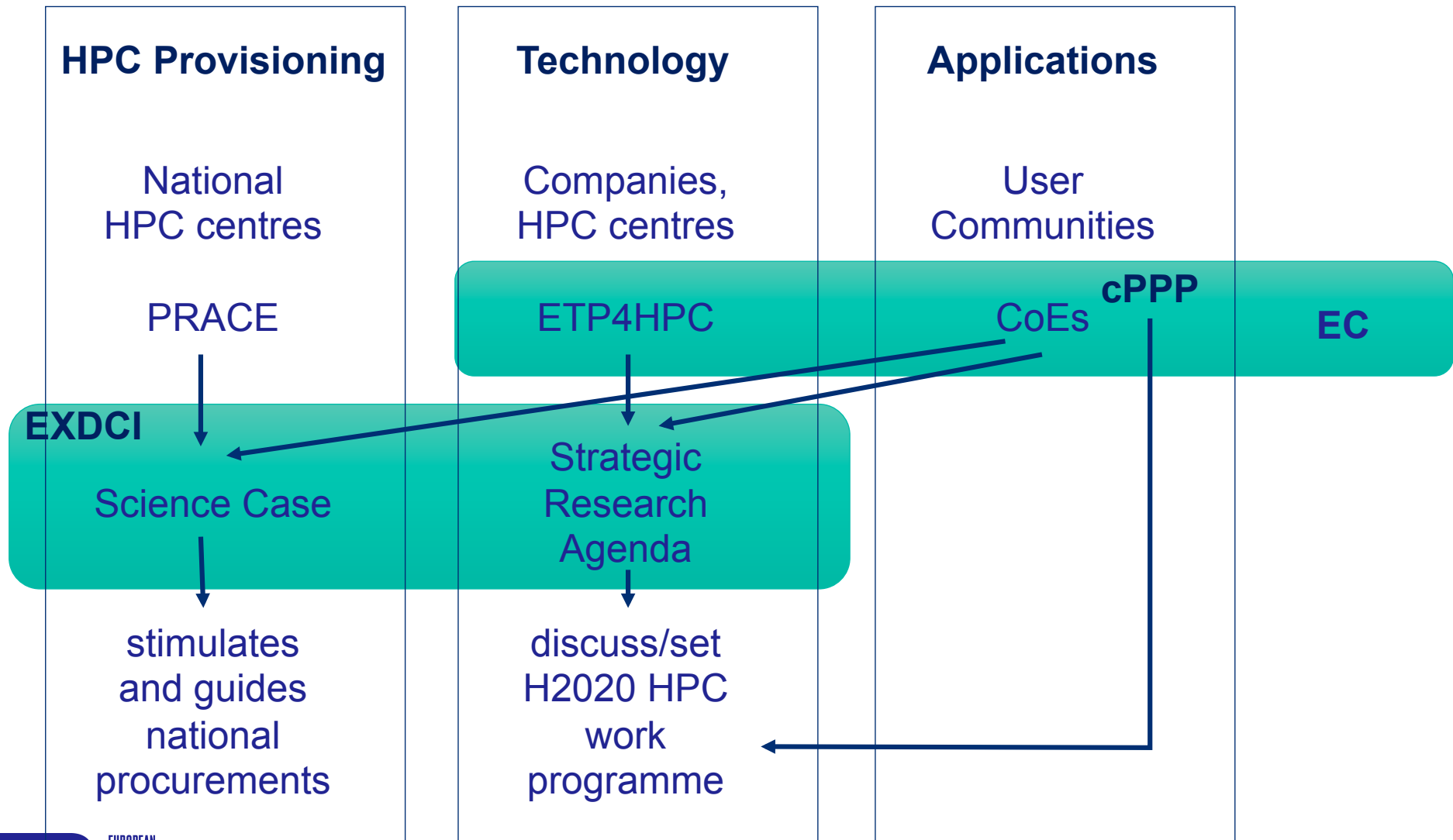
**EUROPEAN TECHNOLOGY  
PLATFORM FOR HIGH  
PERFORMANCE COMPUTING**

# **An Update of the ETP4HPC and Extreme Scale Demonstrators**

**Th.Eickermann, Juelich Supercomputing Centre  
most ETP Slides from Michael Malms**

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# EUROPEAN HPC ACRONYM LANDSCAPE (SMALL EXCERPT)



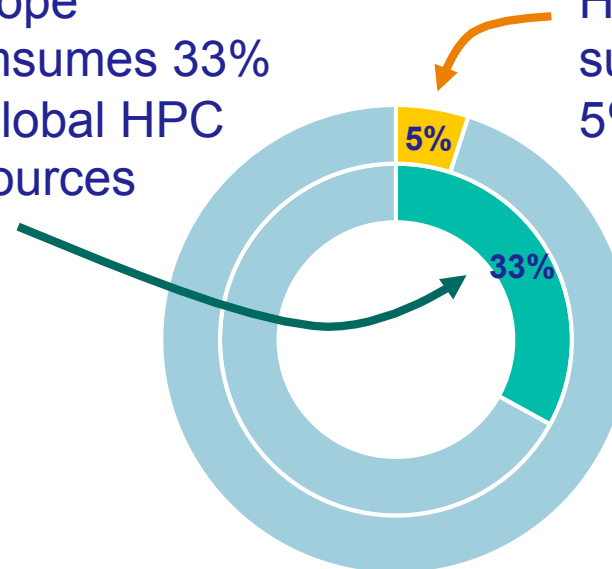
# KEY DOCUMENT: 2012 EC COMMUNICATION

EU needs independent access to HPC technologies, systems and services  
=> ETP4HPC created end of 2012 to contribute to this objective



Europe consumes 33% of global HPC resources

However, supplies less than 5% of them



# SETTING UP THE HPC cPPP

- cPPP signed Dec. 2013 with ETP4HPC (Public-Private Partnership)  
Entry in force Jan. 2014
- Centres of Excellence joined in 2015  
(‘private’ side = ETP4HPC + CoEs)
- Partnership Boards twice a year
- Private side provides input to define H2020 HPC programmes  
which are funded and operated by the EC
- Collaboration with PRACE, BDVA/Big Data PPP  
HiPEAC, Eurolab4HPC...

# OUR ASSOCIATION (DEC. 2017 SNAPSHOT)

## Recent members



2CRSI



ICEOTOPE TECHNOLOGIES LIMITED



PRO DESIGN ELECTRONIC GMBH



HPCNOW!



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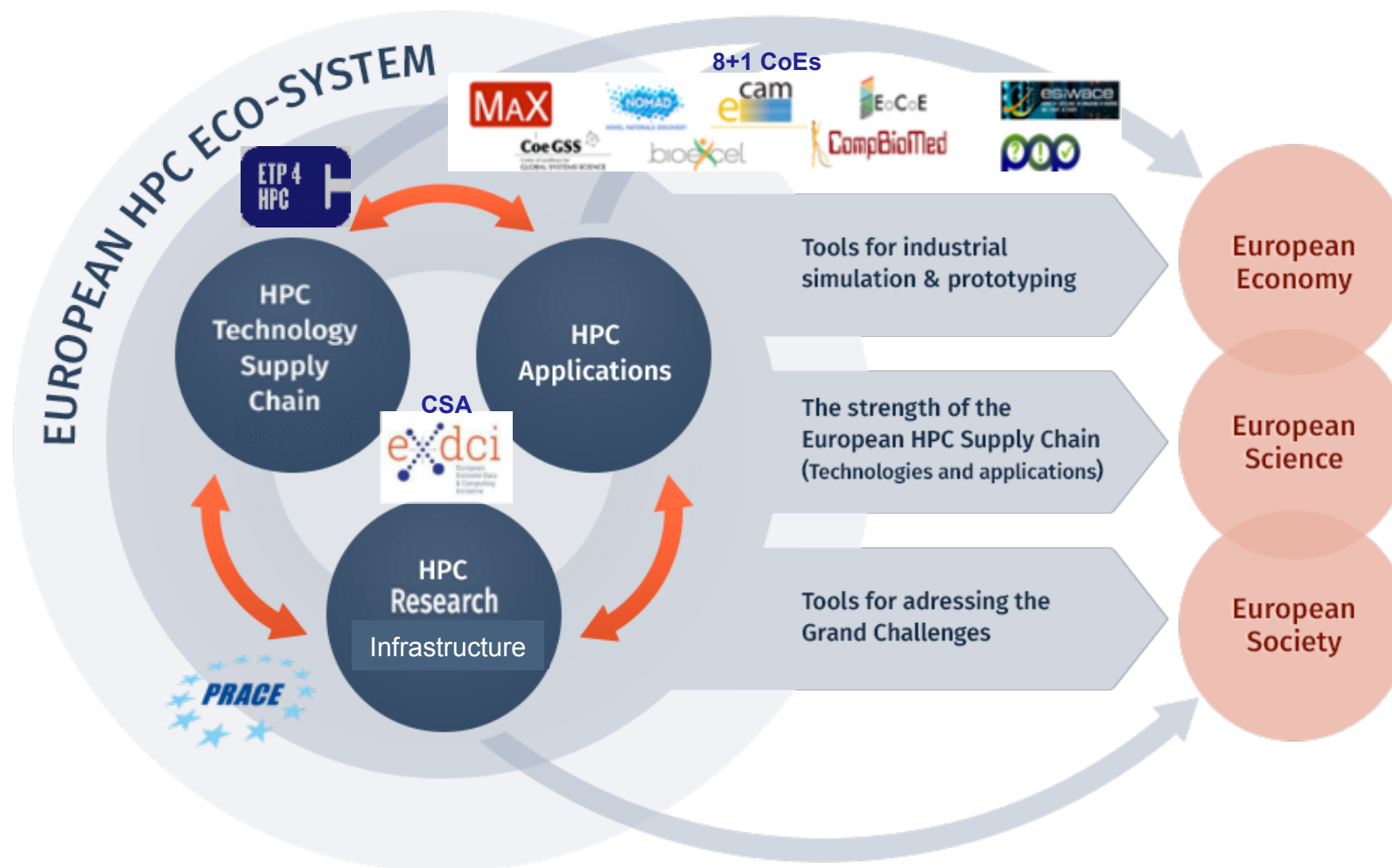
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# EUROPEAN HPC ECOSYSTEM



# ETP4HPC KEY ACTIVITIES

- Foster growth of HPC technology  
Research and Development in Europe
- Advise EC through cPPP
- Define Strategic Research Agenda (SRA)
- Propose H2020 Work Program contents
- Monitor ecosystem development

# ACTIVITIES: SRA3 IN 2017



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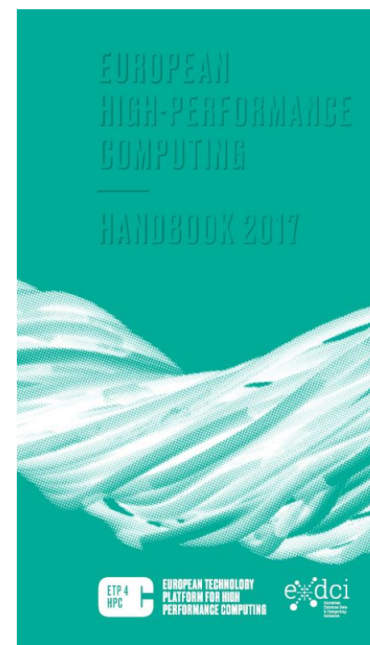
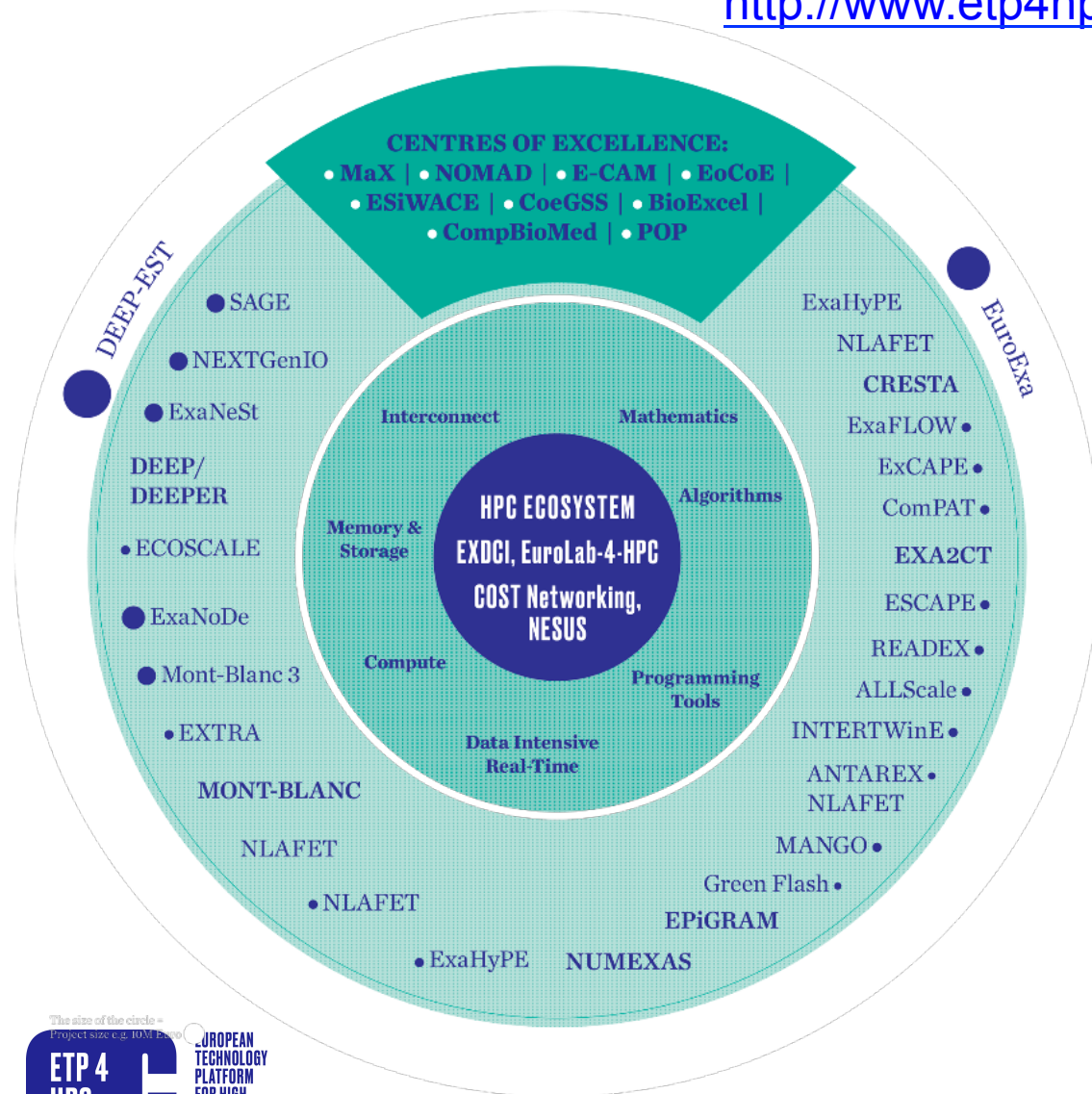
<http://www.etp4hpc.eu/sra.html>



# CURRENT PORTFOLIO

## PROJECTS FUNDED IN 2015-2017

<http://www.etp4hpc.eu/en/european-hpc-handbook.html>



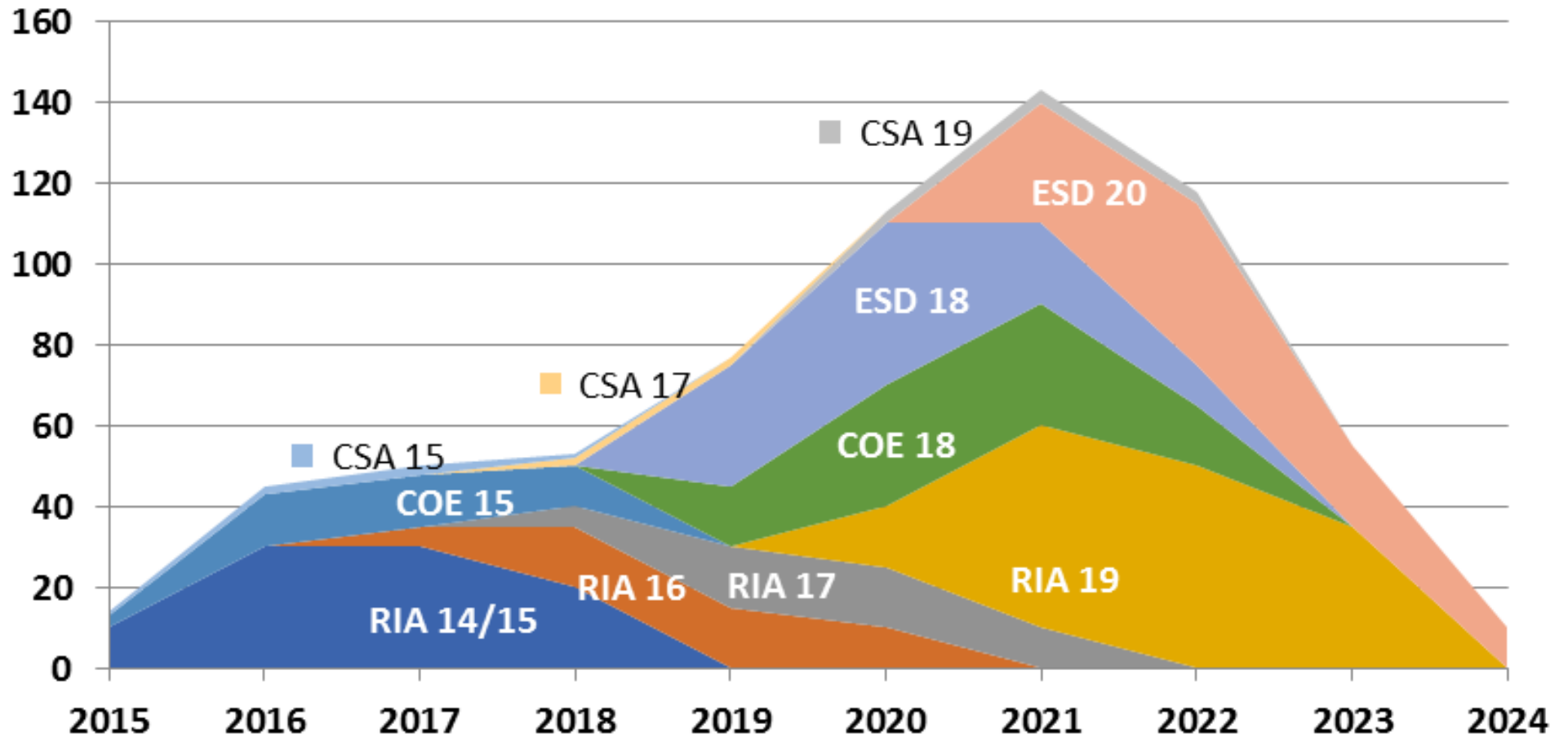
### 2017 EUROPEAN HPC HANDBOOK

Our 2017 European HPC Handbook is available. This professional publication details the HPC Technology and Applications Projects within the European HPC ecosystem. It will be distributed at our Supercomputing 2017 Birds-of-a-Feather Session in Denver (14th Nov 2017, 5.15pm).

If you wish to receive a hard copy, please contact the Office.

# H2020 HPC WORK PROGRAMME – DURATION/VALUES (EURO Ms)

## Funding WP 14-20



ETP4HPC Recommendation

# COMES EUROHPC



EUROPEAN COMMISSION

Press Release Database

[European Commission](#) > [Press releases database](#) > [Press Release details](#)

**European Commission - Press release**

## **Commission proposes to invest EUR 1 billion in world-class European supercomputers**

Brussels, 11 January 2018

**The European Commission unveiled today its plans to invest jointly with the Member States in building a world-class European supercomputers infrastructure.**

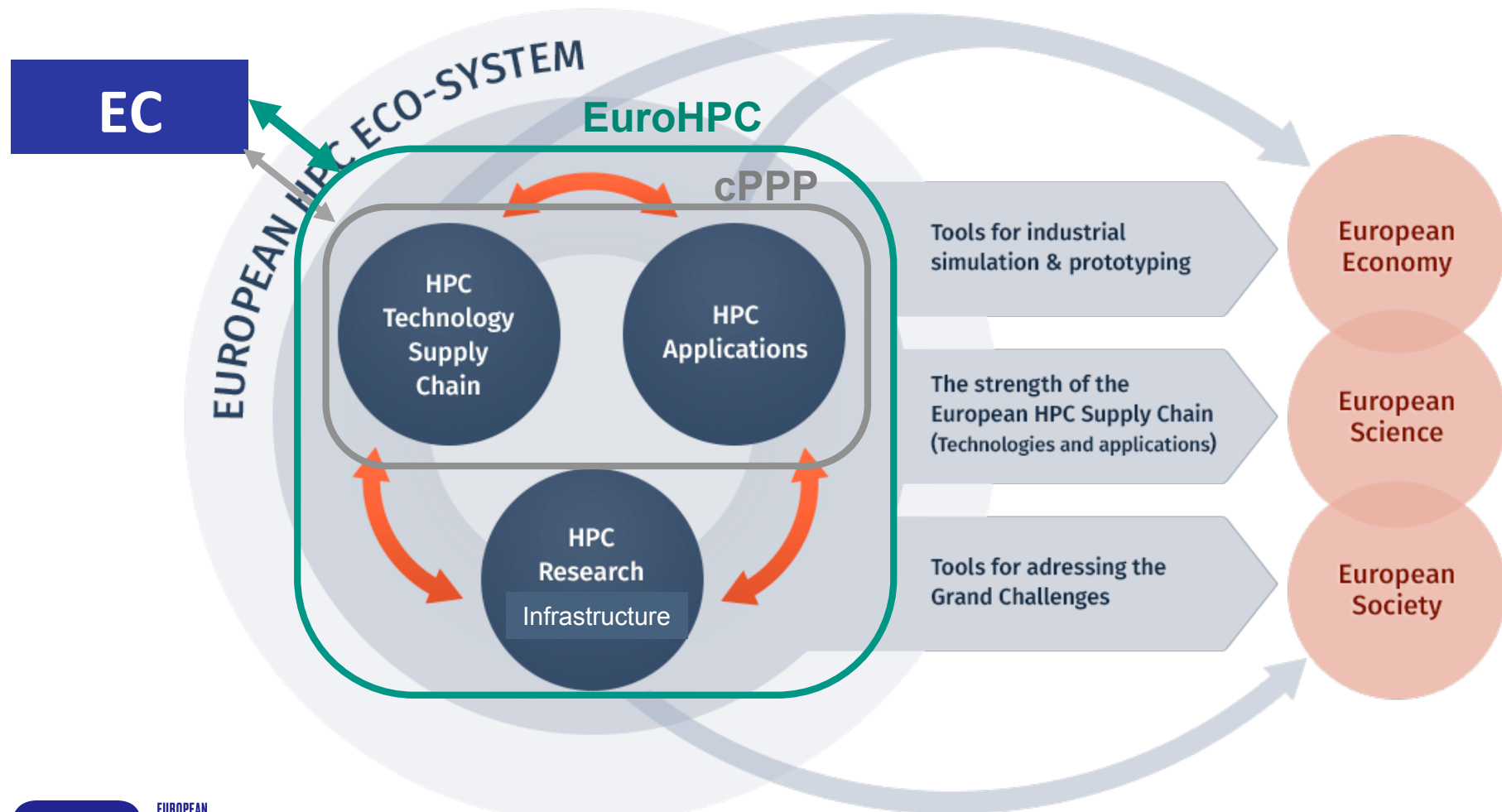
Supercomputers are needed to process ever larger amounts of data and bring benefits to the society in many areas from health care and renewable energy to car safety and cybersecurity.

# EUROHPC MEETING

DG-CNECT/ETP4HPC - 30/01/2018, BRUXELLES

- A large part of the HPC projects under the current **cPPP** will be **transferred to EuroHPC** together with their budget
- DG-CNECT will redirect **486M€** originally earmarked for Work Programme 2019-20 to be managed by EuroHPC (including 10M€ for administration costs). 386M€ coming from the FET, LEIT-ICT and INFRA R&I programmes and an additional 100M€ coming from CEF.
- The **Member States** should contribute to the same amount (**another 486M€**)
- The WP 2019-20 will be updated, dates and some R&I call amounts may be slightly adjusted. Only minor adjustment, no major changes will be possible. The **R&D calls** management will be delegated to **EuroHPC**
- The R&D calls will follow the same rules as currently except that EuroHPC will organize them, not the EC anymore
- Transition period, EuroHPC to take over gradually. E.g. for the European microprocessor FPA, SGA1 (2018) will be handled under current cPPP, SGA2 (2020) by the EuroHPC JU.
- The R&D calls must prepare for **exascale** systems which will be acquired by EuroHPC (call ~2022). This effort encompass Technology, Applications (e.g. the CoEs ), skills development and training.

# FROM CPPP → EUROHPC



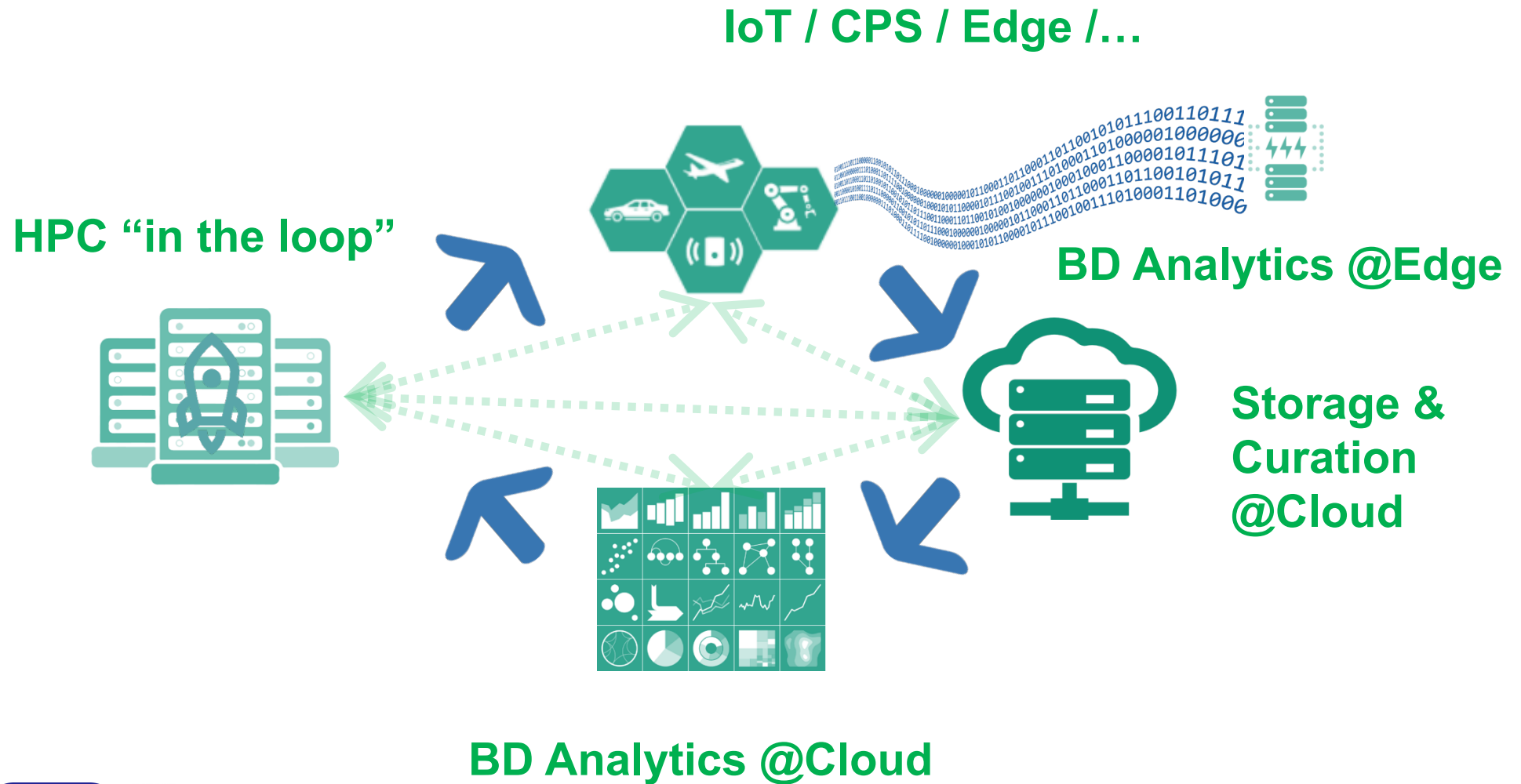
# EUROHPC: A NEW COLLABORATION FRAMEWORK FOR HPC

- EuroHPC is still in definition
- EuroHPC Joint Undertaking is a complex tool

however

- ETP4HPC welcome the EuroHPC initiative
- ETP4HPC role is hardwired into EuroHPC
- EuroHPC opens up some good opportunities
- better coordination and leverage between the different HPC projects
- linking developments (R&I, CoEs) to the exascale (and post-exascale) European infrastructures
- should be flexible enough to grow into new areas

# HPC IN THE LARGER PICTURE





# An Update on Extreme scale Demonstrators

5<sup>th</sup> ENES HPC Workshop on HPC for  
high-resolution climate and weather modelling  
Lecce, May 18th 2018

Thomas Eickermann  
including slides from Marc Durantou



May 18, 2018





# Outline

- Extreme scale Demonstrators in a nutshell
- Preparation – community involvement
- ICT-14-2019 – the call for proposals
- What's next

- Extreme scale Demonstrators – objectives
  - Integrate results of R&D projects into fully integrated systems prototypes
  - Establish proof-points for the readiness, usability and scalability of the technologies
- EsD will fill critical gaps in the HPC H2020 programme:
  - Bring technologies from FET-HPC closer to commercialisation (TRL 7)
  - Combine results from targeted R&D efforts into a complete system (European HPC technology ecosystem)
  - Provide the missing link between the 3 HPC pillars: Technology providers, infrastructure providers, user communities (co-design)

## ***Technology providers***

- Technology integration
- System architects
- Testing and quality/performance assurance (phase A)
- Maintenance and service (phase B)

## ***EsD Expectations***

- Design point 500-1000 PF
- Power efficiency: 35 kW/PF
- Density: 1 PF/rack
- I/O balanced design
- TRL 7

## **EsDs**

## ***Application owners / CoEs***

- Application requirements and key challenges (phase A)
- Port, optimize application(s), use them productively (phase B)

## ***HPC Centres***

- Participate in co-design
- Manage system deployment (phase A)
- System operation, validation (phase B)

# EsDs in a Nutshell: Call for Proposals (#3/3)

## TOPIC : Co-designing Extreme Scale Demonstrators (EsD)

**Topic identifier:** ICT-14-2019

**Publication date:** 27 October 2017

**Types of action:** RIA Research and Innovation action

**DeadlineModel:** single-stage

**Planned opening date:** 26 July 2018

**Deadline:** 14 November 2018 17:00:00

Time Zone : (Brussels time)

- **EsD project structure**
  - **Phase A** (~24 months): Development, Integration and Testing
    - Little or no basic technology research
    - Substantial R&D focus geared towards integrating components and sub-systems developed in the preceding R&D projects
  - **Phase B** (~24 months): Deployment, Benchmarking and Use
    - Operated by a hosting center
    - EsD made available to application owners for code porting and development ... and close-to-production usage
    - Characterization and EsD validation, benchmarking based on real use-cases.

# EsD History

- ETP4HPC created EsD Workgroup in Dec 2014 (after discussions with EC)
- Broad discussion on EsDs in several Workshops:  
(slides and results available at <http://www.etp4hpc.eu/en/esds.html>)
  - EXDCI Workshop '15, Rome: Kick-Off
  - ETP4HPC's SRA2 Nov. '15: introduces EsD
  - HPC Summit '16, Prague: Discuss EsD concept in community and with EC:
    - Technical system characteristics, budget, procurement model, consortia, use cases
  - ISC '16, Frankfurt:
    - focus: from Use Cases to System Specs
  - EXDCI Workshop '16, Barcelona:
    - focus: system integrators & Application Communities
    - gathered input on expectations, interests, constraints, ...
  - cPPP Board meeting, Nov. '16 + EsD Workshop with EC, Dec. 5<sup>th</sup> '16, Brussels
    - Discussion of EsD details

# EsD History (cont.)

- ... Broad discussion on EsDs in several Workshops:
  - HPC Summit Week, May 18th '17, Barcelona
    - EsD Roundtable: final exchange before WP is published & call is opened
  - ISC '17, Frankfurt:
    - Gather input from industrial users
  - Spring / Summer '17
    - Working group drafted EsD chapter for SRA3
  - ETP4HPC's SRA3 public release, Nov '17
  - H2020 Work Programme 2018-2020 release, Oct. 27th, 2017
  - EsD Networking
    - A list of entities indicating their interest in contributing to an EsD consortium: technology providers, HPC-Centres, FETHPC-Projects, CoEs, ...

<http://www.etp4hpc.eu/esd-networking017.html>

# Input from CoEs

- General Requirements
  - EsDs need to be stable enough to allow production runs
  - Clear view on programming models and software stack developments
    - As much as possible, commonly used tools need to be supported (compilers, MPI, OpenMP, numerical libraries, etc.)
    - Novel technologies should provide standard interfaces where possible
  - Applications need to be part of EsD design from the beginning
    - Needs significant engagement from the EsD projects for application porting and optimization
- Open Questions
  - Support for extreme FLOP AND extreme scale data (analytics)
  - How sustainable will novel technologies be (and thus the effort to port)?
  - How will application porting and optimization be funded?
  - Support for ensembles/workflows

extracted from presentation by E.Laure at EsD Roundtable, May '17

## Input from ESiWACE (extracted from a CoE survey)

What are the key scientific challenges and what does it take to achieve them (structured along SRA3 Research Priority topics) ?

- **Architecture:** High bandwidth memory, networks, NVRAM
- **System Software:** Dynamic scheduling, compilers
- **Programming Environment:** Fast standardisation, DSL
- **Energy and resiliency:** Energy aware algorithms
- **Balance Compute, I/O and storage performance:** post-processing on the fly, multi-tier software
- **Big Data and HPC usage models:** Recomputing, data analytics
- **Mathematics and algorithms for extreme scale computing:** disruptive numerical methods (discretisation), data placement

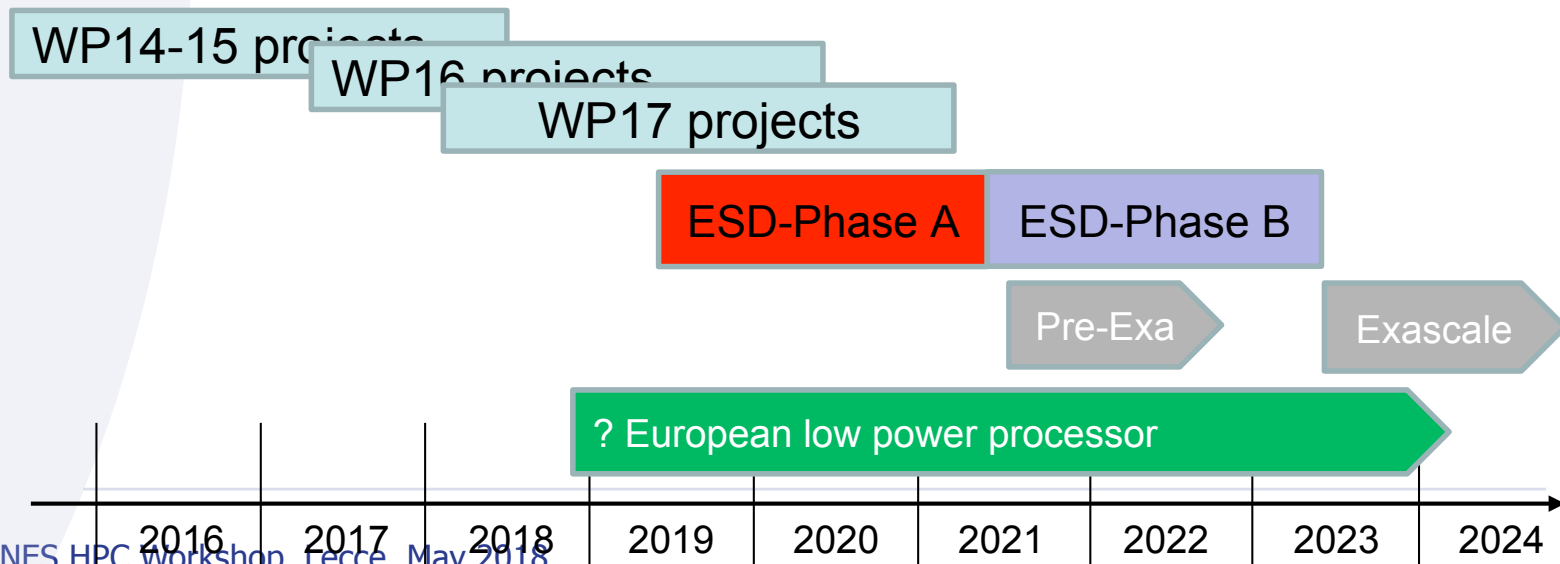


- Call facts
  - Planned timing: 26 July 2018 – 14 November 2018
  - Project start: 1H2019
  - Foreseen funding: 80 Mio. €
  - Anticipated project size: 20 ... 40 Mio. € + national co-funding welcome
- Specific Challenge
  - To demonstrate in operational environments the successful integration of technology building blocks developed in previous R&I actions into world-class Extreme Scale Demonstrators. The challenges of power efficiency, resiliency and scalability of these systems require a **strong co-design approach driven by ambitious applications** involving technology suppliers, system integrators, supercomputing infrastructure providers and **user communities, as well as ambitious HPC and extreme-data application owners or providers.**

... scalability up to exascale-class levels with specific design points and performance/power targets (e.g., 500 Petaflops to 1 Exaflop).

# ICT-14-2018 Co-Designing EsDs cont.

- Further EC expectations expressed in the call text
  - New operational environments and **capacity available for users with extreme-data application requirements**
  - integrate technologies developed in FP7, Horizon 2020 or other R&D actions in Europe, e.g. FETHPC, **LEIT-ICT low-power microprocessor technologies**
  - Proof-of-principle for **pre-exascale machines** addressing strategic HPC and Big-Data applications
  - EC reserves right to block transfer of results to outside EU
- Timeline dependencies



# What's Next

- Challenges for the upcoming EsD projects
  - Balance innovation (based on EU R&D) and stability/usability
  - Timing – how to provide useful input to the Pre-Exascale systems?
  - Manage interests in consortia (integrators, centres, users)
  - Ensure resulting system is no dead-end or one-of system
  - Achieve ambitious goals with a tight budget and schedule
  - Balance budget shares for Technology R&D, Hardware costs, operational costs, application and porting and optimisation
- EsD Working Group mission completed ?
  - Yes, but: ETP4HPC proposed a continuous effort with initially 2 calls
  - ... restart targeting FP9 ?

Thank you for your Attention !

Questions ?

# Backup Slides

# European HPC Strategy in Horizon 2020

